PWM **68**. In response, PWM **68** reduces the pulse width of PWM1 at output **14***a*. The reduction in pulse width of PWM1 reduces the converter channel current flowing through converter channel **18***a* to a value closer to the average of all converter channel currents, as represented by $V_{average}$. Conversely, when converter **10** is operating under, for example, the condition that converter channel **18***b* is carrying a converter channel current that is lower than the average of all converter channel currents, as represented by $V_{average}$, a negative ΔI_2 signal is generated by subtraction circuit **50**. This negativeΔI_2 signal is input into subtraction circuit **60**. Subtraction circuit **60** subtracts the negative ΔI_2 signal from VE/A, i.e. the output of error amplifier **42**, and the output **60***c*, which is electrically connected to input **70***a* of PWM **70**, is increased. In response, PWM **70** increases the pulse width of PWM2 at output **14***b*. The increase in pulse width of PWM2 increases the current flowing through channel **18***b* to a value closer to the average of all converter channel currents, as represented by $V_{average}$.

In the embodiment shown, converter **10** includes four converter channels **18***a*, **18***b*, **18***c*, **18***d*, and control circuit **14** includes four control circuit channels, each including a respective subtraction circuit **48**, **50**, **52**, **54**, another respective subtraction circuit **58**, **60**, **62**, **64**, a respective compensation circuit G1, G2, G3, G4, a respective PWM amplifier **68**, **70**, **72**, **74**, and a respective feedback path **28***a*, **28***b*, **28***c*, **28***d*. However, it is to be understood that converter **10** can be configured to include any number of channels with control circuit **14** be configured with a corresponding number of control circuit channels.

In the embodiment shown, compensation circuits G1, G2, G3, G4 each perform current loop compensation functions, such as, for example, gain or filter functions to shape the current feedback wave, or to prevent current loop instability. However, it is to be understood that it is not always necessary to incorporate compensation circuits into the present invention.

In the embodiment shown, signals $V_{ISENSE1}$, $V_{ISENSE2}$, $V_{ISENSE3}$, and $V_{ISENSE4}$ are proportional to the current in each of feedback loops **28***a*, **28***b*, **28***c*, **28***d*, respectively. However, it is to be understood that the V_{ISENSE} signals may be alternately configured such as being based upon or based partly upon the current carried by the feedback loops, rather than being strictly proportional thereto.

In the embodiment shown, circuits **48**, **50**, **52**, **54**, and circuits **58**, **60**, **62**, **64** are configured as subtraction circuits. However, it is to be understood that each of circuits **48**, **50**, **52**, **54**, and circuits **58**, **60**, **62**, **64** could be alternatively configured, such as, for example, difference amplifiers, to produce an output signal representative of the difference between signals input into the circuits.

While this invention has been described as having a preferred design, the present invention can be further modified within the spirit and scope of this disclosure. This application is therefore intended to cover any variations, uses, or adaptations of the present invention using the general principles disclosed herein. Further, this application is intended to cover such departures from the present disclosure as come within the known or customary practice in the art to which this invention pertains and which fall within the limits of the appended claims.

What is claimed:

1. A multi-phase DC/DC converter having an output voltage, said converter comprising:

a plurality of converter channels, each of said plurality of converter channels including a converter channel input and a converter channel output, each of said plurality of converter channels being configured for generating a converter channel current and for adjusting said converter channel current in response to a control signal electrically connected to each said converter channel input;

a control circuit, comprising:

means for generating an error signal, said error signal being representative of a comparison of said output voltage to a reference voltage;

a plurality of control circuit channels, each of said plurality of control circuit channels corresponding to one of said plurality of converter channels, each of said plurality of control circuit channels comprising:

means for generating a channel current signal, said channel current signal being representative of a corresponding converter channel current;

means for generating a differential channel current signal, said differential channel current signal being representative of a comparison of said channel current signal to an average current signal, said average current signal being representative of an overall average current for said plurality of converter channels;

means for generating a differential error signal, said differential error signal being representative of a comparison of said error signal to said differential channel current signal; and

a pulse width modulator having a ramp input and a control input, said control input being electrically connected to said differential error signal, said pulse width modulator configured for generating said control signal, said control signal being based at least in part upon said differential error signal, said control signal being electrically coupled to a corresponding said converter channel input; and

means for generating said average current signal.

2. The multi-phase DC/DC converter of claim **1**, wherein each of said plurality of control circuit channels further includes a respective compensation circuit.

3. The multi-phase DC/DC converter of claim **2**, wherein each said compensation circuit comprises a frequency compensation circuit having at least one pole and zero, said frequency compensation circuit being configured for at least one of optimizing and stabilizing said differential channel current signal.

4. The multi-phase DC/DC converter of claim **1**, wherein said means for generating a differential channel current signal comprises a first subtracting circuit configured for subtracting said channel current signal from said average current signal.

5. The multi-phase DC/DC converter of claim **1**, wherein said means for generating an error signal comprises an error amplifier having a first input and a second input, said first input being electrically connected to said first input, said second input being electrically connected to a reference voltage.

6. The multi-phase DC/DC converter of claim **1**, wherein said means for generating a differential error signal comprises a second subtracting circuit configured for subtracting said error signal from said differential channel current signal.

7. The multi-phase DC/DC converter of claim **1**, wherein each of said plurality of control circuit channels includes a control circuit channel input, said means for generating a channel current signal comprises a current feedback path, said current feedback path electrically coupling said control

circuit channel input to a corresponding said converter channel output.

8. The multi-phase DC/DC converter of claim 1, wherein said means for generating said average current signal comprises a scaling circuit and a summing circuit electrically connected to said scaling circuit, said summing circuit configured for adding together each respective said channel current signal and for generating a sum signal representative thereof, said scaling circuit configured for scaling said sum signal and for generating said average current signal.

9. A method of balancing a plurality of channel currents, each of said plurality of channel currents flowing in a corresponding one of a plurality of channels in a multi-phase DC/DC converter, said DC/DC converter having an output voltage, said method comprising the steps of: sensing each of said plurality of channel currents to thereby determine a plurality of channel current signals;

averaging together said plurality of channel current signals to thereby determine an average channel current signal;

comparing each of said plurality of channel current signals to said average channel current signal to thereby determine a respective differential channel current signal for each of said plurality of channels;

further comparing said output voltage to a reference voltage to thereby determine an error signal;

furthermore comparing each said differential channel current signal to said error signal to thereby determine a respective differential error signal for each of said plurality of channels; and

adjusting each of said plurality of channel currents based at least in part upon a corresponding said differential error signal to thereby make each of said plurality of channel currents substantially equal to each other.

10. The method of claim 9, comprising the further step of stabilizing and optimizing said differential channel current signal.

11. The method of claim 10, wherein said stabilizing and optimizing step comprises filtering each said differential channel current signal with a frequency compensation circuit, said frequency compensation circuit having at least one pole and zero.

12. The method of claim 9, wherein said averaging step comprises:

adding with a summing circuit each of said plurality of channel current signals to thereby produce a summing signal; and

scaling said summing signal with a scaling circuit to thereby produce said average channel current signal.

13. The method of claim 9, wherein said comparing step comprises subtracting with a subtracting circuit said average channel current signal from each of said plurality of channel.

14. The method of claim 9, wherein said further comparing step comprises subtracting with a subtracting circuit said reference voltage from said output voltage of said converter.

15. The method of claim 9, wherein said furthermore comparing step comprises subtracting with a subtracting circuit said error signal from each said differential channel current signal.

16. The method of claim 9, wherein said adjusting step comprises electrically coupling a respective one of each said differential error signal to an input of a corresponding pulse width modulator, each said pulse width modulator configured for issuing a control signal, each said control signal based at least in part upon a corresponding said differential error signal, each said control signal being electrically coupled to a corresponding one of said plurality of channels, each of said plurality of channels being configured for adjusting a corresponding one of said plurality of channel currents based at least in part upon said control signal to thereby make each of said plurality of channel currents substantially equal to each other.

17. A multi-phase DC/DC converter, comprising:

a converter output;

a plurality of converter channels, each of said plurality of converter channels having a respective converter channel input and a respective converter channel output, each said converter channel output being electrically connected to said converter output, each of said plurality of converter channels being configured for sourcing a respective channel current, each of said plurality of converter channels being configured to adjust a corresponding said channel current in response to a control signal electrically connected to a corresponding said converter channel input; and

a control circuit, comprising:

a summing circuit having a plurality of summing circuit inputs and a summing circuit output;

a plurality of current feedback paths, each of said plurality of current feedback paths electrically connecting a respective said converter channel output to a corresponding one of said plurality of summing circuit inputs;

a scaling circuit having a scaling input and a scaling output, said scaling input being electrically connected to said sing circuit output;

a plurality of first subtraction circuits each having a first input, a second input and a first subtraction circuit output, each said second input being electrically connected to said scaling output, each said first input being electrically connected to a corresponding one of said plurality of current feedback paths;

an error amplifier having a reference input, an error input, and an error output, said reference input being electrically connected to a reference voltage;

a voltage feedback path connecting said converter output to said error input of said error amplifier;

a plurality of second subtraction circuits each having a first input, a second input and a second subtraction circuit output, each said first input being electrically connected to said error output, each said second input being electrically connected to a corresponding said first subtraction circuit output; and

a plurality of pulse width modulators each having a ramp input, a control input, and a pulse width modulator output, each said control input being electrically connected to a corresponding said second subtraction circuit output, each said ramp input being connected to a ramp voltage source, each said pulse width modulator output being electrically connected to a corresponding said converter channel input.

18. The DC/DC converter of claim 17, further comprising a plurality of frequency compensation circuits each having an input and an output, each said input being electrically connected to a corresponding said first subtraction circuit output, each said output being electrically connected to a corresponding said second input of one of said plurality of said second subtraction circuits.

* * * * *